An IF Digital Down-Converter for Software Radio DVB-S2 Receivers

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***Abstract*— The second generation of DVB specs, DVB-S2, was developed for satisfying the today's needs for reliable and effective broadband satellite communication services even under 'hostile' conditions. This is achieved by exploiting the new advances in the fields of coding and modulation. Software defined radio (SDR) proves to be an enabling technology for future multimode and reconfigurable satellite receivers. This work presents the design and implementation of a new digital down-converter (DDC) architecture that can be integrated into the next generation software radio DVB-S2 receivers. The presented DDC module is based on two cascaded stages of frequency conversion, operating on samples fed by an A/D converter of moderate sampling frequency. The DDC contains also a sample rate conversion subunit which performs decimation on the resulting in-phase and quadrature (I/Q) samples for proper interfacing with demodulator logic at lower rates. The presented DDC has been implemented and tested using field programmable gate arrays (FPGA), while its performance has been evaluated under additive white Gaussian noise and for various DVB-S2 modulation schemes.**

I. Introduction

Many technological innovations have taken place in the field of digital communications in the last decade, especially in error correcting and modulation. The capabilities arised by the use of new error correcting schemes, have paved the way for more effective and more reliable communications, even in 'hostile' channels. Additionally, the increasing demand for supporting more efficient existing and future applications and services, over wide bandwidth satellite transponders, led to the development of the new spec for broadband satellite communications, DVB-S2 [1]. The scope of this new spec is to replace the previous and for many years globally deployed DVB-S, as it is able to effectively exploit the available space segment resources, while giving the opportunity to older DVB-S terminal receivers to continue their operation [2].

DVB-S2 was developed in order to provide high performance broadcasting and unicasting applications, which are related to power and spectral adaptivity at reasonable receiver complexity. These characteristics are based on the versatility provided by the DVB-S2 physical layer, providing a variety of modulation and coding schemes that are able to change on a frame-by-frame basis, according to channel conditions. Inevitably, the flexibility of DVB-S2 systems and the evolutionary trends in digital communications systems affect the design approaches and methods in satellite receivers.

At the same time, software defined radio (SDR) is a promising technology that enables, the required adaptivity and reconfigurability through the support of multiple operational modes and data rates, along with the ability to integrate new functions in existing designs. The SDR concept is related with the advances in A/D converter technology, in terms of higher sampling rates and resolution, which helps digital signal processing to expand towards the antenna by minimizing traditional analog components such as channel filters, frequency mixers e.t.c. These technological advances give the designers the ability to realize flexible and versatile digital receivers that can handle IF signals with proper digital processing techniques [3].

Combining these tendencies, this paper focuses on the design and implementation of a digital down-converter module that can be used in software radio DVB-S2 IF receivers. The module receives a digitally sampled IF signal, centered at 70 MHz, and generates two data streams representing the in-phase and quadrature signal components. The 70 MHz IF frequency comprises a standard value utilized by many modulator and demodulator platforms in the DVB-S2 equipment market. The key feature of the presented DDC module is that it uses two cascaded frequency conversion submodules with fixed and programmable carrier frequency respectively, while it requires samples from an A/D converter of a moderate rate.

Section II gives an overview of the SDR based DVB-S2 terminal IF receiver that utilizes the proposed DDC architecture and presents in details the DDC functionality. In Section III the implementation of the DDC module in an FPGA device is outlined. Finally, based on experimental results, Section IV demonstrates the performance of the implemented down-converter using various metrics.

II. The SDR DVB-S2 Receiver and the DDC Architecture

Figure 1 presents the architecture of a software radio DVB-S2 IF receiver. The down-converter is the first digital processing unit of the receiver that processes IF signals and converts them into the respective baseband signals, by using two cascaded stages of frequency conversion. The digital samples at the DDC output, comprising the in-phase and

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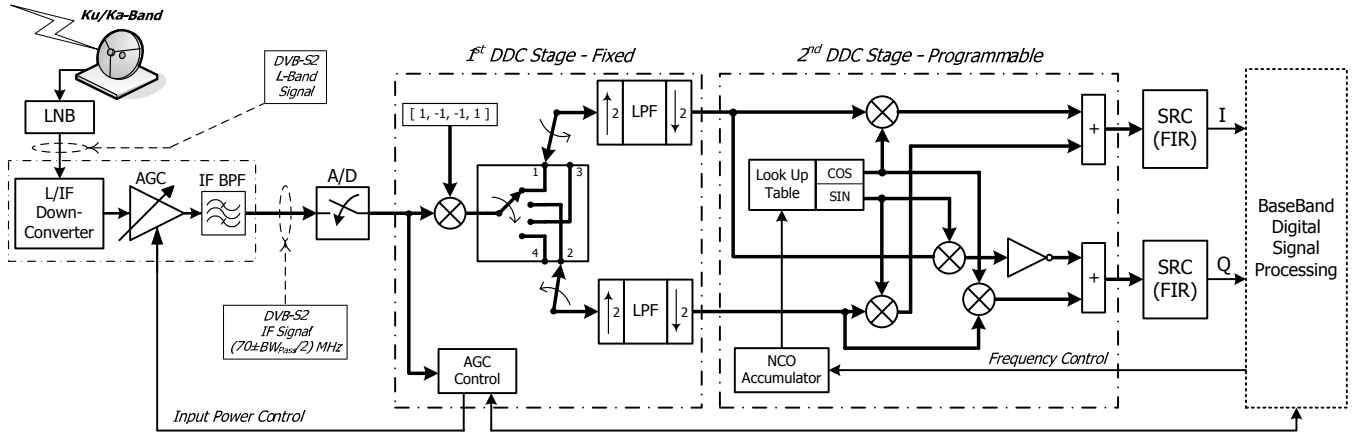

Fig. 1. SDR DVB-S2 Receiver and the IF Digital Down-Converter

quadrature signal components, are fed to the baseband digital processing circuits, where synchronization, demodulation and decoding is performed.

The received RF signal (Ku or Ka band) is downconverted to the L-band, using an out-door Low Noise Block (LNB). Afterwards, the signal is further converted to the IF band (around $F_c = 70$ MHz in our case) by an analog down-converter module that includes output power control and bandpass filtering. Power control is achieved by using an Automatic Gain Controller (AGC) that is driven by measurements performed inside the DDC module using the A/D samples in order to adjust the received signal to the dynamic range of the A/D converter. The AGC also includes a fixed bandwidth bandpass filter. If BW_{Pass} (in MHz) is the bandwidth of this bandpass filter, the maximum supported symbol rate R_s (in MBaud) is given by:

$$R_s \leq \frac{BW_{Pass}}{(1+\alpha)} \tag{1}$$

where α is the roll-off factor as specified by the DVB-S2 standard (0.20, 0.25 or 0.35).

The IF signal is sampled by an ADC at a rate of F_s (in MSps), which is chosen so as to satisfy the Nyquist criterion and be k times the symbol rate R_s of the received signal, that is:

$$\begin{gathered} 2(F_c + BW_{Pass}/2) \leq F_s \ \leq F_{ADC} \\ F_s = k \cdot R_s \text{ and } k = \text{even integer} \end{gathered} \tag{2}$$

where F_{ADC} is the maximum sampling rate of the used ADC.

The selection of the even factor k is strongly related to the sample rate conversion (SRC) stage at the DDC output. Given the ADC sampling frequency F_s, the first step of the DDC processing is the mixing of the sampled signal with a quadrature oscillator of a fixed frequency $F_s/4$. This is typically managed by multiplying the ADC samples with the periodic sequences {1, 0, -1, 0} and the {0 , -1, 0, 1} in the real and imaginary path respectively. Given an input sample sequence $\{in_1, in_2, in_3, in_4...\}$, after multiplication the results of the two paths would be $\{in_1, 0, -in_3, 0...\}$ for real and $\{0, -in_2, 0, in_4...\}$ for the imaginary respectively, so we alternatively multiply the input samples with the periodic sequence {1 , -1, -1, 1} and feed the real branch with the first and third sample and the imaginary with the second and fourth, thus the sequences become $\{in_1, -in_3...\}$ and $\{-in_2, in_4...\}$ respectively. Thus both signal component paths operate at half the ADC sampling rate and no multiplier is required [3]. Then, zeros are inserted between the samples of both signal components and the quadrature is delayed by a sample period relative to the in-phase one. Afterwards both channels are low pass filtered in order to suppress the unwanted signal images of higher frequencies. At the filter output a down-sampler by a factor of 2 is applied in order to recover the initial sampling rate ($F_s/2$).

The next processing stage is a programmable frequency converter that utilizes a numerical control oscillator (NCO) and a complex multiplier, with both running at $F_s/2$ MHz. The NCO generates the samples of an arbitrary frequency complex carrier, while a complex multiplier performs the mixing of the incoming samples with the respective carrier samples. The functionality of this stage is based on a phase accumulator register that produces suitable phase arguments that are mapped to samples of a prestored sinusoid waveform in a look-up table, according to a frequency control input. The NCO frequency resolution Δf (in Hz) is determined by the running clock frequency ($F_s/2$) and the number of bits (B) of the phase accumulator register, as:

$$\Delta f \text{ (Hz)} = \frac{F_s/2}{2^B} = \frac{F_s}{2^{B+1}} \tag{3}$$

Therefore, the output frequency of the NCO for a given input u (unsigned value) to the phase accumulator, is given by:

$$f_{NCO} \text{ (Hz)} = \frac{F_s \cdot u}{2^{B+1}}, \quad u \in [0, 2^{B-1} - 1] \tag{4}$$

Finally, after this complex multiplication, a sample rate conversion (SRC) takes place, that provides the necessary rational rate-change factor so that the sampling rate of the DDC output is adjusted to an integer multiple of the nominal

symbol data rate. Usually, baseband units operate at 2, 4 or 8 times the symbol data rate. The rate conversion mechanism combines a polyphase FIR interpolation filter with the appropriate decimator at its output, which keeps the clock of each polyphase subfilter to $F_s/2$. The complexity of the SRC stage plays a significant role in the selection of the even integer k (eq. 2) for a given ADC maximum sampling rate, seeking for the smallest integer factors for interpolation and decimation procedures.

III. The DDC Implementation

The presented down-converter has been implemented on a VirtexII-Pro device (XC2VP30), which was interfaced with a 12-bits A/D converter of 210 MSps maximum sampling frequency. In this section, we present details of the DDC implementation according to the following parameters: 70 MHz IF carrier frequency, 10 MBaud symbol rate, roll-off factor 0.35 and 36 MHz passband bandwidth of the external L-band to IF down-converter. The ADC sampling rate was set to 200 MSps (20 times the symbol rate) which results to 100 MSps per channel. The clock of the first conversion stage was set to 50 MHz, which transfers the IF signal down to 20 MHz. After interpolation and low pass filtering at 200 MSps, both signal components are downsampled back to 100 MSps. The filtering operation at the fixed stage is performed by a lowpass FIR filter of 40 taps with 31.75 MHz -3dB bandwidth which is determined by the signal's maximum frequency (26.75 MHz) and the maximum carrier uncertainty (5 MHz in DVB-S2).

The next DDC subsystem, which comprises the programmable frequency conversion stage, converts the signal down to baseband by using a complex carrier locally generated by an NCO running at 100 MHz clock frequency. The accumulator length of the NCO is chosen to be 18 bits wide, which provides a frequency resolution of 381.469 Hz. Due to the frequency offset at the input of the frequency converter, the NCO is set to generate a complex carrier at 20 MHz. Given the NCO running clock frequency and the accumulator's length, the best control value corresponds to 20.00007629 MHz frequency providing a total residual frequency offset at baseband of 76.29 Hz (almost 1ppm). Finally, a polyphase filter converts the sampling rate to four times the symbol rate, based on a lowpass FIR filter of 32 taps and -3dB bandwidth of 11.75 MHz, which includes the previously described carrier frequency uncertainty. The used interpolation to decimation factor ratio is set to 2/5.

Table I presents the allocation of the FPGA resources to the various processing stages of the implemented DDC system on the XC2VP30 VirtexII-Pro Xilinx device in percentages (numbers inside parenthesis correspond to the absolute resources). As it is shown, Fixed DC and SRC stages utilize significantly more resources than the Programmable DC, which is strongly affected by the existence of FIR filters.

Resources (%)	Fixed DC	Program. DC	SRC	Total
SLICEs	22 (3055)	3 (406)	37 (5106)	62 (8567)
Flip-Flops	21 (5733)	1 (264)	34 (9506)	56 (15503)
LUTs	15 (4162)	2 (653)	27 (7462)	44 (12277)
RAMB16s	0	3 (4)	0	3 (4)

TABLE I
VirtexII-Pro (XC2VP30) resource utilization percentages per processing stage.

IV. Experimental Results

In this section we present various experimental results that depict the performance and the efficiency of the proposed DDC in conditions of additive white Gaussian (AWG) noise and for various DVB-S2 modulation schemes. Theses measurements are performed using the DDC parameters outlined in Section III. The modulated signal at the L-band is generated by a programmable Vector Signal Generator that drives the external 'L-band to IF' down-converter, which provides the input signal for the ADC. In order to properly perform the required measurements, carrier frequency and symbol timing are recovered and a demodulator including matched filtering and de-mapping operations is attached to the DDC output for retrieving the randomly transmitted symbols. For measuring the DDC performance, Modulation Error Ratio (MER) (dB) and Error Vector Magnitude (EVM) (%) are used [4]. These performance metrics are defined as follows:

$$MER = 10\log_{10}\frac{\sum_{j=1}^{N}(I_j^2+Q_j^2)}{\sum_{j=1}^{N}[(I_{R_j}-I_j)^2+(Q_{R_j}-Q_j)^2]} \quad (5)$$

and

$$EVM = \frac{\sqrt{\frac{1}{N}\sum_{j=1}^{N}[(I_{R_j}-I_j)^2+(Q_{R_j}-Q_j)^2]}}{\frac{1}{N}\sum_{j=1}^{N}\sqrt{(I_j^2+Q_j^2)}}\times 100 \quad (6)$$

As a reference signal we used the in-phase and quadrature component values we recover at a high performance Vector Signal Analyzer attached to the output of the 'L-band to IF' down-converter, in the absence of noise. These reference signals are determined as I_j and Q_j respectively, while a large number, N, of randomly transmitted symbols has been used. The respective values taken after carrier-symbol recovery and matched filtering operations on the samples coming from the DDC output are specified as I_{R_j} and Q_{R_j}. Initially, we calculated these two metrics without any additional noise in order to determine the effect of the used fixed-point arithmetic on the performance of the proposed DDC. The introduced normalized magnitude error for the various DVB-S2 modulation schemes follows the gaussian distribution with zero mean and variances: $2.558{\cdot}10^{-4}$ for QPSK, $2.525{\cdot}10^{-4}$ for 8PSK, and $3.70{\cdot}10^{-4}$ for 16APSK. Similarly, the introduced phase error (in degrees) follows also the gaussian distribution with zero mean and variances: 0.77081 for QPSK, 0.77084 for 8PSK, and 1.67261 for 16APSK.

Figures 2 and 3 show the measured *MER* and normalized *EVM* values in the presence of AWGN for the cases of QPSK, 8PSK and 16APSK. The QPSK and the 8PSK modulation schemes demonstrates almost the same performance since all

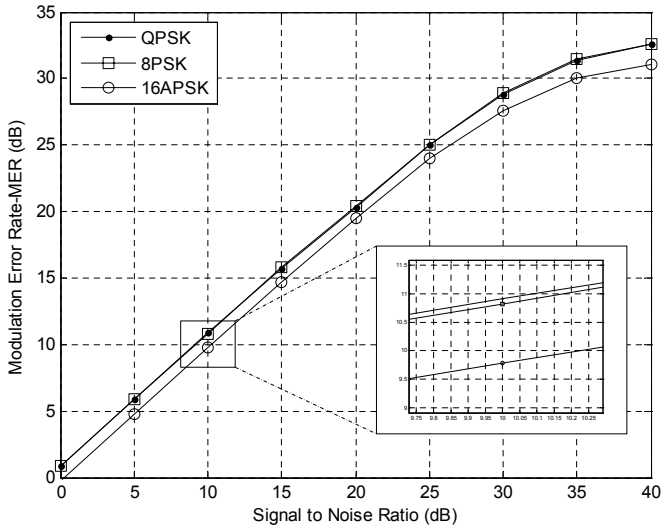

Fig. 2. MER for QPSK, 8PSK and 16APSK DVB-S2 modulation schemes.

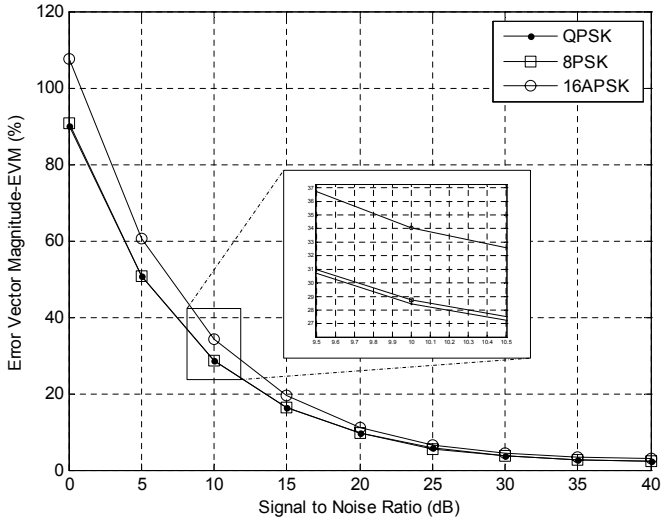

Fig. 3. EVM for QPSK, 8PSK and 16APSK DVB-S2 modulation schemes.

points of both constellations are on the same ring, with 8PSK being slightly more sensitive to phase errors. Since 16APSK allocates its constellation points into two modulation rings and smaller amplitude is used in the inner ring, the EVM increases compared to the other constant envelop schemes. Finally, Figures 4 and 5 highlight the effect of AWGN in the case of QPSK and 16APSK, by using the cumulative distribution functions (CDF) of normalized magnitude and phase errors. Again, the 16APSK (red lines) is more sensitive to the noise conditions, especially in terms of phase noise since a much denser constellation, compared to QPSK, is used.

V. Conclusion

In this work, an IF digital down-converter (DDC) architecture has been presented and analyzed, which comprises a suitable solution for software radio DVB-S2 receivers that use A/D converters of moderate sampling frequency.

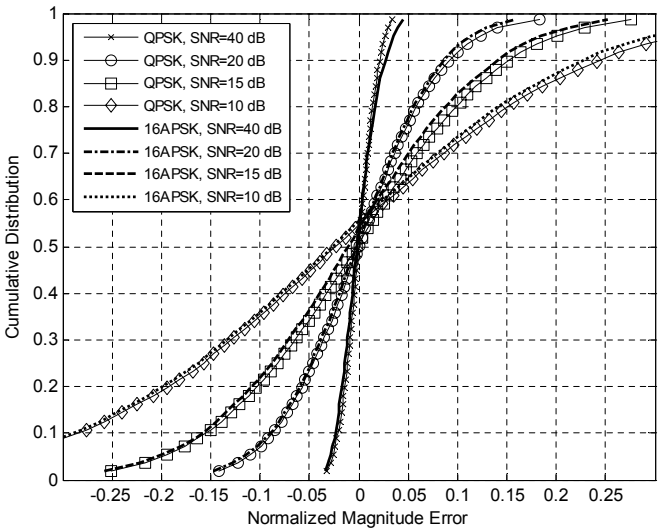

Fig. 4. Normalized Magnitude Error CDF of QPSK and 16APSK modulation schemes under AWG noise.

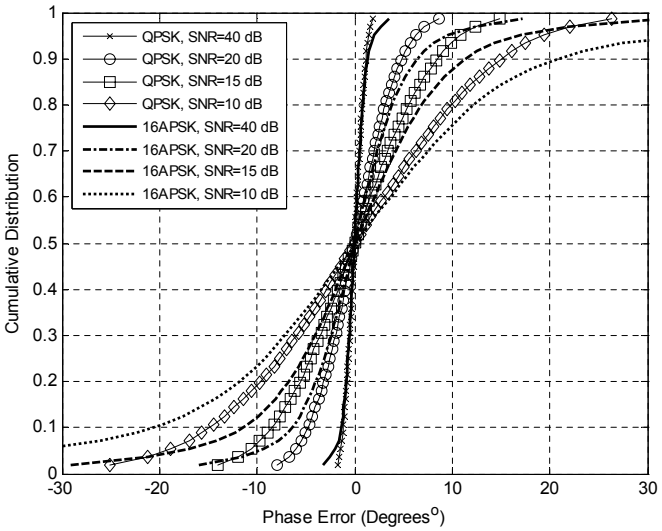

Fig. 5. Phase Error CDF of QPSK and 16APSK modulation schemes under AWG noise.

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