COMPARATIVE PERFORMANCE ANALYSIS OF SYMBOL TIMING RECOVERY FOR DVB-S2 RECEIVERS

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Abstract

The need for reliable broadband satellite communication services has led to the development of the second generation DVB spec, DVB-S2. This paper considers the performance of a feedback Symbol Timing Recovery technique, which is based on the Non-Data-Aided (NDA) Gardner Timing Error Detector (TED), in an all-digital DVB-S2 IF receiver architecture. The Symbol Timing Recovery performance is measured in terms of lock-in time and estimation accuracy, with the contribution of simulation results over all different modulation schemes used by the DVB-S2 standard (QPSK, 8PSK, 16APSK and 32 APSK) and under noise sources such as non-linearities, additive white Gaussian noise (AWGN) and significant residual carrier frequency offset.

1. Introduction

New technologies have been presented in the field of digital communications in the last decade, especially in modulation and forward error correction. The capabilities arised by the use of these new schemes, have paved the way for more reliable and more effective communications, even under extremely hostile channel conditions. The growing demand for more efficient digital satellite communications services and applications led to the development of the second generation DVB specification for broadband satellite communications, DVB-S2 [1]. The scope of this new specification is to gradually replace the older and for many years globally deployed DVB-S, as it is able to effectively exploit the available space segment resources while it provides the opportunity to older DVB-S receivers to continue their operation. DVB-S2 was developed in order to provide high performance in broadcasting and unicasting applications, which are totally based on power and spectral adaptivity at reasonable receiver complexity. These characteristics are achievable due to the versatility of the DVB-S2 physical layer that utilizes a variety of modulation and error coding schemes according to channel conditions. As a consequence, new DVB-S2 terminal receivers need to operate at low signal-to-noise ratios (SNRs) and non-linearities which is also a major concern for the satellite communications system designers.

This work deals with a symbol timing recovery (STR) mechanism used in DVB-S2 receivers [2], which is a second order close-loop based on the non-data-aided (NDA) Gardner timing error detector (TED) [3]. This scheme combines structural simplicity along with the capability to operate at all different DVB-S2 modulation formats, under even a significant residual carrier frequency offset. According to these features, STR has to be able to converge without prior precise carrier synchronization, thus comprising the first synchronization procedure performed in typical DVB-S2 receivers. Based on these aspects, this paper presents the configuration and setup approach for second order closed-loop STR techniques based on the NDA Gardner TED, as a part of an all digital IF DVB-S2 receiver including a digital down converter (DDC) module operating at 70 MHz. Apart from designing aspects, a thorough performance analysis, in term of lock-in time and estimation accuracy, is also given under different channel conditions including non-linearities, AWG noise and residual carrier frequency offset. The functional verification as well as the performance evaluation is performed through extensive simulations based on digital samples of captured DVB-S2 IF signals of all different modulation formats (QPSK, 8PSK, 16APSK, 32 APSK) from a DVB-S2 compliant modulator, a high level impairments model (non-linearities or AWG noise) and the all-digital DVB-S2 IF receiver architecture consisting of DDC and STR subunits.

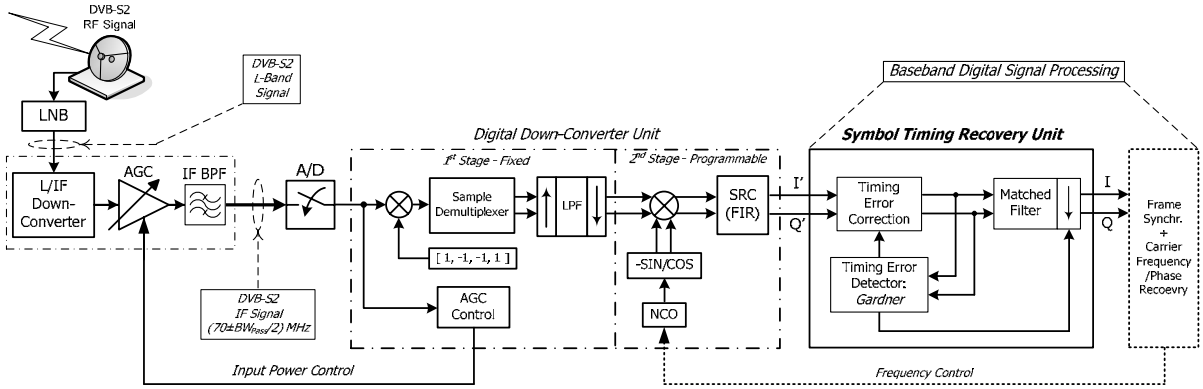

Figure 1: A DVB-S2 Receiver Architecture

Section 2 gives an overview of the all-digital IF DVB-S2 terminal receiver architecture, while Section 3 highlights the design and parameterization of the closed-loop STR technique. Section 4 presents the measurement platform, the used performance metrics and the respective performance results.

2. The DVB-S2 IF Receiver

A DVB-S2 receiver consists of an out-door unit (parabolic antenna and LNB), an external L to IF down converter and an all-digital IF receiver, as shown in Figure 1. The all-digital IF receiver uses an A/D converter, driven by a free running oscillator, for digitizing the incoming signal and the digital samples feed the first digital processing unit, the digital down-converter (DDC). DDC converts the IF signals into baseband signals, through two cascaded stages of frequency down-conversion. The DDC output samples, in the form of in-phase and quadrature signal components, are used by the baseband digital processing circuits for synchronization, demodulation and decoding. The first task performed inside the baseband processing unit is the symbol timing recovery (STR), which is implemented as a second order loop before the matched filter, generates samples synchronized to the incoming symbols, which are used by the subsequent modules for frame, carrier and phase synchronization and decoding purposes.

The incoming RF signal (at Ku/Ka band), is initially down-converted to the L-band, using the LNB of the out-door unit, and then the signal is further down-converted to the IF-Band (F_c = 70 MHz center frequency) by an analog down-converter module that includes output power control and bandpass filtering operations. Incoming signal adjustment is achieved by an automatic gain controller (AGC), implemented in the digital down-converter (DDC) of the IF digital receiver. The AGC is driven by a power measurement circuit implemented in the DDC, in order to properly adjust the received signal to the dynamic range of the used ADC. The AGC also includes a fixed bandwidth bandpass filter. If BW_{Pass} is the bandwidth of the bandpass filter (in MHz), the maximum supported symbol rate R_s (in MBaud) is given by:

$$R_s \leq \frac{BW_{Pass}}{(1+\alpha)} \tag{1}$$

where α is the roll-off factor supported by the DVB-S2 standard (0.20, 0.25 or 0.35).

The IF signal is sampled by the ADC at a rate of F_s (in MSps), which is chosen so as to satisfy the Nyquist criterion and be k times the symbol rate R_s of the received signal, that is:

$$\begin{gathered} 2(F_c + BW_{pass}/2) \leq F_s \leq F_{ADC} \\ F_s = k \cdot R_s \end{gathered} \tag{2}$$

where k is an even integer and F_{ADC} is the maximum sampling rate of the used ADC. The selection of the even factor k is strongly related to the sample rate conversion (SRC) stage at the DDC output. Given F_s, the first step of the DDC processing is to mix the sampled signal with a quadrature oscillator of a fixed frequency $F_s/4$. This is typically managed by multiplying the ADC samples with a periodic sequence resulting to two signal components of half the ADC sampling rate ($F_s/2$) [4]. As the actual sampling rate is recovered, both signals are low pass filtered in order to suppress the unwanted signal images at higher frequencies and at the filter output a down-sampler is applied.

The next processing stage is a programmable frequency down-converter that utilizes a numerical control oscillator (NCO) and a complex multiplier, with both running at $F_s/2$. The frequency down-converter is controlled by a carrier recovery second order loop, which is initiated after STR and frame synchronization convergence. The functionality of this stage is based on a phase accumulator register that produces suitable phase arguments that are mapped to samples of a pre-stored sinusoid waveform in a look-up table, according to a frequency control input. The NCO frequency resolution Δf (in Hz) is determined by the running clock frequency ($F_s/2$) and the number of bits (B) of the phase accumulator register, according to:

$$\Delta f = \frac{F_s/2}{2^B} = \frac{F_s}{2^{B+1}} \tag{3}$$

Therefore, the output frequency of the NCO for a given input u (unsigned value) to the phase accumulator, is given by:

$$f_{NCO} = \frac{F_s \cdot u}{2^{B+1}}, \qquad u \in [0, 2^{B-1} - 1] \tag{4}$$

Finally, at the DDC output, sample rate conversion (SRC) takes place, that provides the necessary rational rate-change factor so that the sampling rate of the DDC output is adjusted to an integer multiple of the actual symbol data rate. The rate conversion mechanism combines a polyphase FIR interpolation filter with the appropriate decimator at its output, which keeps the clock of each polyphase subfilter to $F_s/2$. The complexity of the SRC stage plays a significant role in the selection of the even integer k of the equation (2) for a given ADC sampling rate, seeking for the smallest integer factors for interpolation and decimation procedures. The NDA closed-loop STR technique presented in the next section, requires that the sample rate at the DDC output is 2 or 4 times the symbol rate.

3. Closed-Loop STR technique based on the NDA Gardner TED

This section presents the architecture of the digital STR feedback loop, which is shown in Figure 2, and performs initial acquisition and tracking of the actual symbol rate by using an estimate of the timing error given by the Non-Data-Aided (NDA) Timing Error Detector (TED) proposed by Gardner [3]. The elements comprising the STR loop are the Gardner TED, the first order loop filter and the Farrow structured digital interpolator along with its control logic (Timing-NCO). Matched filtering and the respective down-sampling is performed on the samples generated by the STR loop. All elements within the feedback loop contribute to the symbol synchronization process. Timing error is estimated by the Gardner TED in an average rate equal to the actual symbol rate and then is filtered by the loop filter, whose output drives the control logic of T-NCO. Finally, the interpolator is controlled by the T-NCO, and that results to the minimization of the detected timing error.

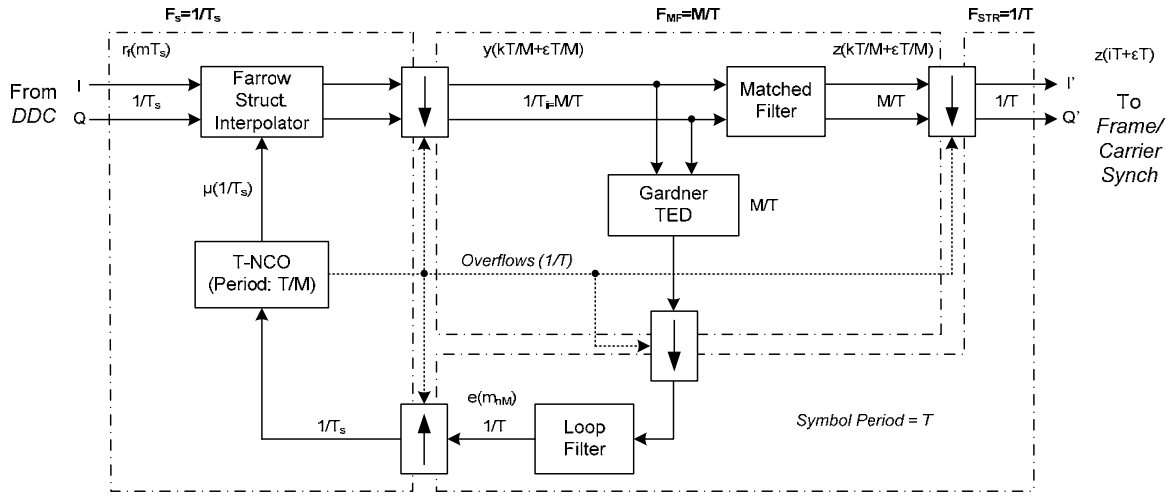

Figure 2: Closed-Loop STR using the NDA Gardner TED

3.1 Interpolation Filter

The function of the interpolation filter is to calculate a sample $y(kT_i)$ using a set of adjacent input samples $x(mT_s)$, and a fractional interval μ ($0 \le \mu \le 1$) which both are obtained from the T-NCO control logic, explained in a following subsection. T_s comprises the sampling period of the input stream, derived from the DDC output and T_i the period of the interpolated samples. Based on the fact that after the interpolator the NDA Gardner TED is used, which needs two samples per symbol for its timing error detection, T_i equals to T/M, where T indicates the actual symbol period and M is an integer number 2 or 4. A well known architecture used in timing recovery applications utilizes a piecewise polynomial interpolator [5] structure which provides a great balanced trade-off between efficient hardware implementation and performance. The fundamental equation for digital interpolation is given by the following equations:

$$y(kT_i) = y[(m_k + \mu_k)T_s] = \sum_{i=I_1}^{I_2} x[(m_k - i)T_s] \cdot h_I[(i + \mu_k)T_s] \quad (5)$$

where $x(m)$ are the input samples and $h_I(t)$ is a finite duration impulse response of a time continuous interpolation filter. Farrow implementation assumes that the impulse response is a piecewise polynomial in each T_s interval, with index i being in the interval [I_1, I_2], (I_1, I_2 integer numbers). Practically, basepoint index m_k identifies the $I=I_2-I_1+1$ signal samples to be used for the kth output y and fractional interval μ_k identifies the I coefficients employed in equation (5) for the generation of kth output y. Equation (5) can be written as a nested and more efficient representation in terms of implementation, which for cubic Farrow structure, used in our case, is:

$$y(k) = [\{u(3)\mu_k + u(2)\}\mu_k + u(1)]\mu_k + u(0) \quad (6)$$

where:

$$u(n) = \sum_{i=I_1}^{I_2} b_n(i)x(m_k - i) \quad (7)$$

Coefficients b_n are constants, independent of μ_k, solely determined by the filter's impulse response $h_I(t)$. There are total $N \cdot I$ coefficients if all impulse-response segments are described by polynomials of the same degree N. In the case of the cubic interpolator, N=3 which represents the polynomial's degree. Cubic Farrow structure includes 4 columns of FIR transversal filters of fixed coefficients. Each FIR column has $I=4$ taps. The coefficients of cubic interpolator columns are given in [5].

3.2 NDA Gardner TED

The basic element of the STR loop is the timing error detector (TED). Gardner's TED comprises an NDA algorithm that is proposed for use in DVB-S2 symbol synchronizers due to its independence from the received data symbols and the carrier frequency errors. The Gardner TED requires two samples for every incoming symbol. The extraction of the timing error for the kth data symbol is given by:

$$e_k = y_i(kT - \frac{T}{2})\{y_I[(k-1)T] - y_I(kT)]\} + y_Q(kT - \frac{T}{2})\{y_Q[(k-1)T] - y_Q(kT)]\} \quad (8)$$

The S-curve of the TED is computed by closely following the derivation of [6], and using the equation:

$$S(\delta) = \frac{4C_{const}K}{T}\sin(\frac{2\pi\delta}{T}) \quad (9)$$

where $\delta=\tau-\hat{\tau}$ (τ : actual timing error, $\hat{\tau}$: estimated value) and assuming independent random data symbols $\{c_i\}$ from an alphabet of size N with zero-mean:

$$E\{c_i c_k^*\} = \begin{cases} C_{const}, & i = k \\ 0, & i \neq k \end{cases} \quad (10)$$

Parameter K is given by the following integral, in which $H(f)$ is equal to the root-raised cosine pulses function (in frequency domain):

$$K = \int_{-\infty}^{\infty} H(\frac{1}{2T} + f)H(\frac{1}{2T} - f)\cos(\pi fT)df \quad (11)$$

as TED is applied directly before the matched filtering operations, and equals to:

$$K = \frac{\alpha}{\pi(\alpha^2 - 1)}\cos(\frac{\pi\alpha}{2}) \quad (12)$$

Equations (12) and (9) indicate that the S-curve is a sinusoidal function of period T (symbol period) and passes from the origin when $\delta=0$. The curve amplitude is proportional K and also a function of the roll-off factor α. From the amplitude of the S-curve we can determine the gain K_D of the Gardner TED which is equal to $4C_{const}K \cdot 2\pi$.

3.3 Proportional-Integral First Order Loop Filter

The loop filter plays a significant role in the STR loop since it determines its loop bandwidth, B_LT, which is strongly related to the required lock-in time and the estimation accuracy during the acquisition and tracking modes, respectively. The loop filter also characterizes the order of the STR loop. In order to design a second order feedback loop, a well known first order PI (Proportional-Integral) loop filter is used, whose transfer function equals to:

$$F(z) = \frac{g_0 + g_1 z^{-1}}{1 - z^{-1}} \tag{13}$$

where the filter coefficients g_0 and g_1 are given by:

$$g_0 = \frac{1}{K_D K_0}\left(\frac{\alpha_1}{\alpha_0} + 2\right) \qquad \text{and} \qquad g_1 = \frac{1}{K_D K_0}\left(\frac{\alpha_2}{\alpha_0} - 1\right) \tag{14}$$

K_D and K_0 are the gains of TED and T-NCO, respectively. Parameters α_0, α_1, α_2 are obtained from the discrete time second-order PLL model, which results to:

$$\alpha_0 = 4(\omega_n T)^2 + \zeta\omega_n T + 4\,, \quad \alpha_1 = 2(\omega_n T)^2 - 8\,, \quad \alpha_2 = 4(\omega_n T)^2 - \zeta\omega_n T + 4 \tag{15}$$

ω_n stands for the natural frequency (rad/sec) and ζ for the damping factor ($0<\zeta<1$) and is usually set to $1/\sqrt{2}$. The configuration of the loop filter is based on the normalized to the symbol rate loop bandwidth parameter, which for second order feedback loops the respective natural frequency is given by:

$$B_{L,2} = \frac{1}{2}\omega_n\left(\zeta + \frac{1}{4\zeta}\right) \tag{16}$$

The loop filter bandwidth determines the STR accuracy and acquisition time. The higher the bandwidth, the faster the acquisition process but with less accurate results. In order to achieve a faster circuit with increased accuracy, the implemented STR uses two loop filters with different loop bandwidths, one wide and one narrow, and a control circuit that determines which filter is used as the time progresses. Both filters are always fed with new samples, but their outputs are swithced in order to drive the T-NCO. The above approach achieves to accelerate the acquisition process in order for the feedback loop to result to an error signal in the vicinity of the real error and at this point the output of the filter with the narrower loop bandwidth is used for achieving sufficient estimation accuracy. The STR loop starts its operation with the loop filter associated with the wider loop bandwidth and if the normalized timing error, which feeds T-NCO, maintains the '*same*' mean value (over a number of samples determined by the narrow loop bandwidth $1/(2\cdot B_L T_{LOW})$) in a specific range for a period of time, the narrower filter gets the control of the loop.

3.4 Interpolator Control Logic (T-NCO)

TED produces an error signal at symbol rate 1/T using fractionally spaced samples $kT_i=kT/M$ (M integer). In our case M can be either 2 or 4. Since the sampling rate $1/T_s$ is not an exact multiple of the symbol rate, samples of period T_i need to be mapped onto the time scale of STR loop input samples of period T_s. This is expressed as:

$$kT_i + \varepsilon_i T_i = L_{INT}[kT_i + \varepsilon_i T_i]T_s + \mu_k T_s = m_k T_s + \mu_k T_s \tag{17}$$

$L_{INT}(x)$: largest integer ≤ x

For every input sample, control logic computes the corresponding basepoint m_k and the fractional delay μ_k in order to obtain the respective interpolated values. A new sample is inserted into the Farrow structure everyT_s, while a new output is computed at each basepoint m_kT_s. This procedure explains the decimator appearing at the output of the interpolator in Figure 2. Due to the fact that the error signal at the TED is produced at symbol rate, a second decimation needs to be performed which selects every Mth basepoints m_k $(k=nM)$ to output one error signal. The previous decimator is also

depicted in Figure 2. Afterwards the TED signal is processed by the loop filter, whose output $e(m_{nM})$ is used to adjust the control word $w(m_{nM})$ of the T-NCO.

$$w(m_{nM}) = w(m_{(n-1)M}) + K_0 e(m_{(n-1)M}) \tag{18}$$

where in our case $K_0=1$.In the absence of noise the control word assumes its correct value:

$$w = \frac{T_i}{T_s} = \frac{1}{M}\left(\frac{T}{T_s}\right) \tag{19}$$

Basepoint and fractional delay are computed recursively as follows: Using equation (17), the next sample $(k+1)T_i+\varepsilon_i T_i$ is given by:

$$(k+1)T_i + \varepsilon_i T_i = m_k T_s + \mu_k T_s + T_i = m_k T_s + (\mu_k + \frac{T_i}{T_s})T_s \tag{20}$$

If the unknown ratio is replaced with the estimate $w(m_k)$ (equation (19)) then is obtained:

$$(k+1)T_i + \varepsilon_i T = m_k T_s + L_{INT}[\hat{\mu}_k + w(m_k)]T_s + [\hat{\mu}_k + w(m_k)]_{mod1} T_s \tag{21}$$

and finally, the estimates of m_k and μ_k are given by:

$$\begin{aligned} m_{k+1} &= m_k + L_{INT}[\hat{\mu}_n + w(m_k)] \\ \hat{\mu}_{n+1} &= [\hat{\mu}_n + w(m_k)]_{mod1} \end{aligned} \tag{22}$$

4. Performance Results

In this section, various performance results are presented which depict the behaviour of the previously described STR feedback loop, over several impairments encountered in forward satellite channels. The most significant impairment found in such a channel is related to the non-linearities introduced by the Travelling Wave Tube Amplifier (TWTA) of the satellite transponder. Additionally, since the STR loop is the first synchronization mechanism activated in a DVB-S2 receiver after power up, residual carrier frequency offset is also an important peculiarity that is regularly added to the previous conditions and needs to be studied how it affects the performance of the STR mechanism. Apart from non-linearities and frequency offset, additive white Gaussian noise is also considered.

The performance metrics used for studying the STR behaviour under the above channel conditions are the initial acquisition time (*lock-in* time) and the accuracy of the symbol rate estimation error during tracking. As lock-in time we consider the time required to achieve the steady-state for the first time. The second metric is the RMS value of the normalized estimated timing error.

All performance results have been derived from a measurement setup, which is based on off-line processing using real samples from a DVB-S2 compliant transmission signal. The setup consists of a DVB-S2 compliant IF (70 MHz) modulator, a hardware platform with a high-speed ADC and a large storage memory and a high level model describing the channel impairments (AWGN or non-linearities) along with the all-digital IF DVB-S2 receiver described in Section 2. The DVB-S2 IF modulator was used in order to generate the respective signal for all different modulation formats (different MODCODs) including also the impairment of the residual carrier frequency error. Concerning the high level model of non-linearities, we have utilized the AM/AM and AM/PM characteristics of the Hellas-SAT 2 [7]. All experiments have been performed with the following parameters: Nominal Symbol Rate: 10 MBaud, roll-off 0.35, M=2 (at the cubic interpolator), wide normalized loop bandwidth 10^{-4}, narrow loop bandwidth $5\cdot10^{-5}$.

Figures 3(a) and 3(b) depict the RMS estimation accuracy and the required acquisition time in the presence of AWG noise respectively, for all modulation schemes and for zero frequency offset error. As the first figure demonstrates, the RMS estimation accuracy improves as the noise level decreases while it is slightly affected by the different modulation schemes. The acquisition time is slightly affected by the increase of noise power for all modulation schemes, but it is increased as the size of the used constellation increases. Figure 3(c) presents the RMS accuracy in relation to carrier frequency offset error at a given AWG noise level (E_s/N_0=20dB). As it is shown, the RMS accuracy is not affected significantly either by the frequency offset error or the used constellation. On the other hand, Figure 3(d) shows how the frequency offset affects the acquisition time for all different modulation schemes. More populated constellations introduce longer acquisition time in contrast to less populated due to the fact that the Gardner TED generates an increased error signal as the average distance between the received symbols becomes larger.

Figures 3(e) and 3(f) present the RMS accuracy and acquisition time in the presence of non-linearities for zero frequency offset, respectively. Under this impairment, the RMS accuracy is strongly affected by small changes of the Output Back Off (OBO) parameter in the non-linear area, for all modulation schemes. Additionally, there is a significant difference between the RMS values reached by two ring modulations (16APSK and 32APSK) compared to single ring modulations (QPSK and 8PSK), due to smaller distances between adjacent symbols. The same conclusion is also derived from the acquisition time figure that shows a more significant increase in the acquisition time for 16APSK and 32APSK, in the same window of OBO values. From both figures it is evident that for OBO higher than -2dB, 16APSK and 32APSK fail to lock in contrast to the other constellations. Figures 3(g) and 3(h) show that for -6dB OBO level, the RMS accuracy is not affected by the increase of frequency offset error in contrast to the acquisition time which is affected significantly. Furthermore, QPSK and 8PSK have better acquisition time and RMS accuracy as they are more robust in non-linear conditions.

5. Conclusions

In this paper, an STR feedback loop utilizing the well known NDA Gardner TED was thoroughly presented and analysed as a part of an all-digital DVB-S2 IF receiver. A detailed analysis for the STR loop configuration was presented along with information for each loop component, while extensive measurements were used for performance evaluation in terms of lock-in time and estimation accuracy in initial acquisition and tracking respectively. The impairments considered during the experiments were non-linearities, AWG noise and residual carrier frequency offset.

6. Acknowledgment

This work was supported by the European Regional Development Fund (ERDF) and the Greek Ministry of Development – General Secretariat for Research and Technology (GSRT).

7. References

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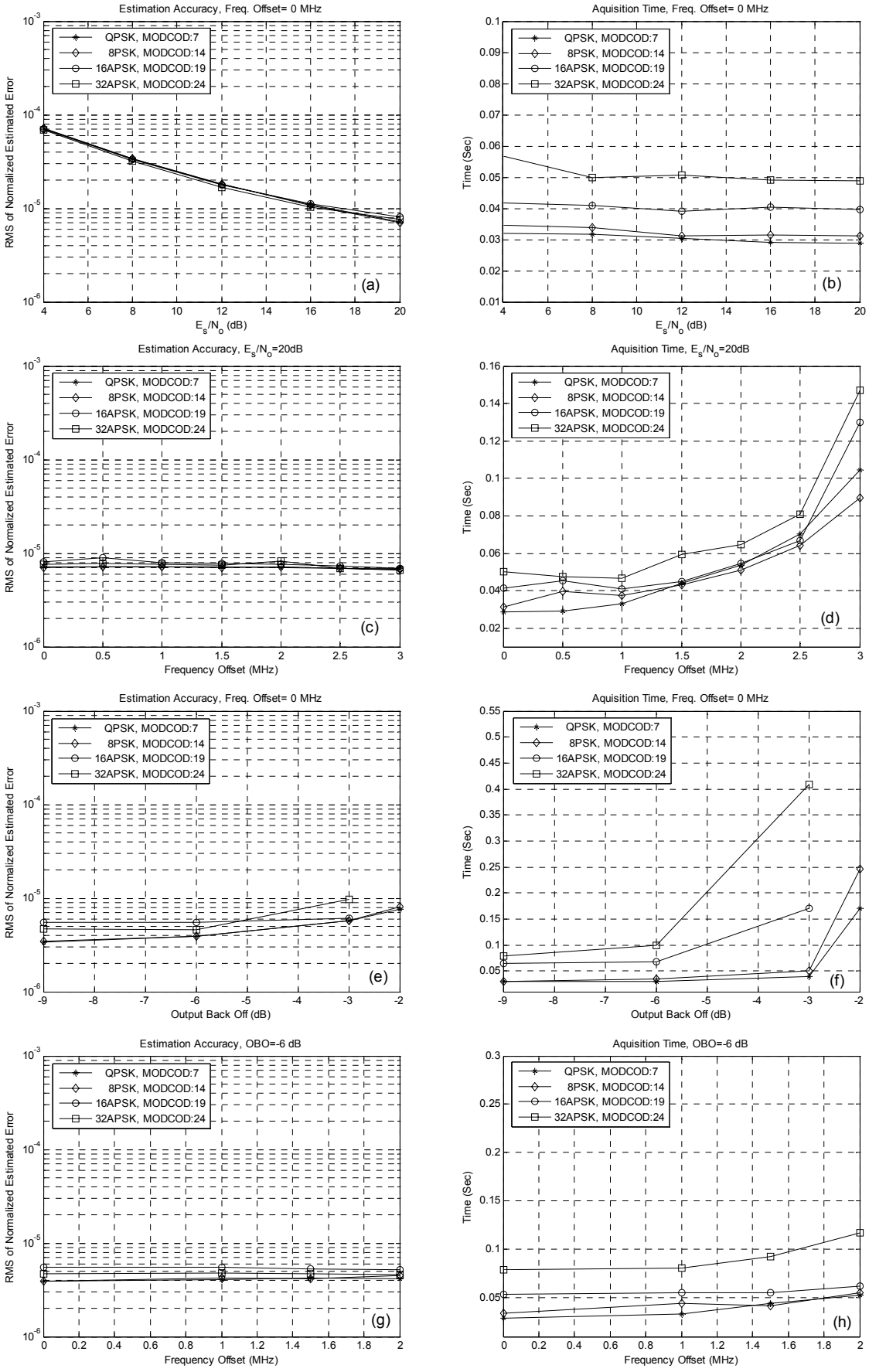

Figure 3: STR Performance Metrics under different impairments