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ADSL Binder Modeling: Signaling and Data Transmission

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Abstract

This paper presents a simulation model of a binder of asymmetric digital subscriber lines (ADSL). The model is developed in the Simulink environment and enables the investigation of multicarrier communication aspects in the complex system of a loop binder interconnecting the customer premises with the nearby central office. Key features of the model architecture are the update of the model block parameters during simulation and the interconnection of the simulation environment with a reprogrammable hardware platform that facilitates the substitution of selected model components with prototype circuit modules. The mixed-level setup of the ADSL binder model and the hardware platform constitutes a versatile environment for the development and investigation of new single-modem and/or centralized algorithms for the ADSL technology.

1. Introduction

The digital subscriber line (DSL) [1] technology is the industry solution to the *last mile* problem. New generation DSL modems can provide high-speed data communication services in the order of Mbps, over the twisted-pair cables. In contrast to the voice-band modems, the DSL transceivers utilize higher frequencies for data exchange by applying advanced coding and signal processing techniques. Due to the increasing demand for higher data rates and the need for new broadband services, DSL technology has attracted a lot of attention over the last 10 years.

Asymmetric digital subscriber line (ADSL) [2] technology is one of the most well established technologies for data communication services over the twisted-pair cable infrastructure. ADSL uses a form of multicarrier transmission, known as Discrete Multitone (DMT) [3], which decomposes the channel spectrum into 256 narrowband subchannels of 4.3125 kHz bandwidth each. Commercial ADSL modems provide up to 6 Mbps in short loops and 1.5 Mbps in long loops [4].

In this paper we present the simulation model of a binder of ADSL lines. The model was developed in the Simulink environment and enables the analysis of the ADSL transmission in a subscriber loop binder interconnecting the customer premises (CP) with the nearby central office (CO). Figure 1 shows the basic architecture of such a DSL system. In contrast to the end-to-end dial-up connections of the voice-band modems, the DSL communication requires a DSL modem pair between each CP side and the local CO. Due to the utilization of high frequencies, the noise environment of the DSL binder is very severe [5] and crosstalk interference induced by neighboring lines is one of the largest noise impairments that reduce system performance. Crosstalk is characterized as near-end crosstalk (NEXT) generated by transmitters located at the receiver's side and far-end crosstalk (FEXT) generated by transmitters at the opposite side of the receiver. Our simulation model incorporates analytical modeling of the crosstalk coupling between the ADSL lines based on the transmission characteristics of each transceiver pair.

The development of methods for achieving coordination among the DSL modems in order to improve the total binder

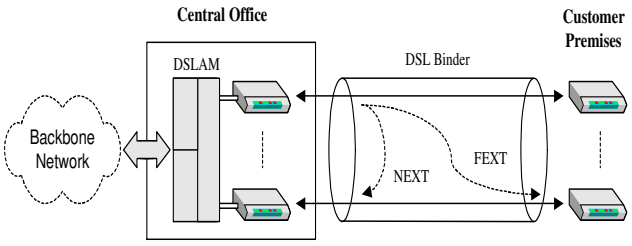

Figure 1. The DSL system architecture.

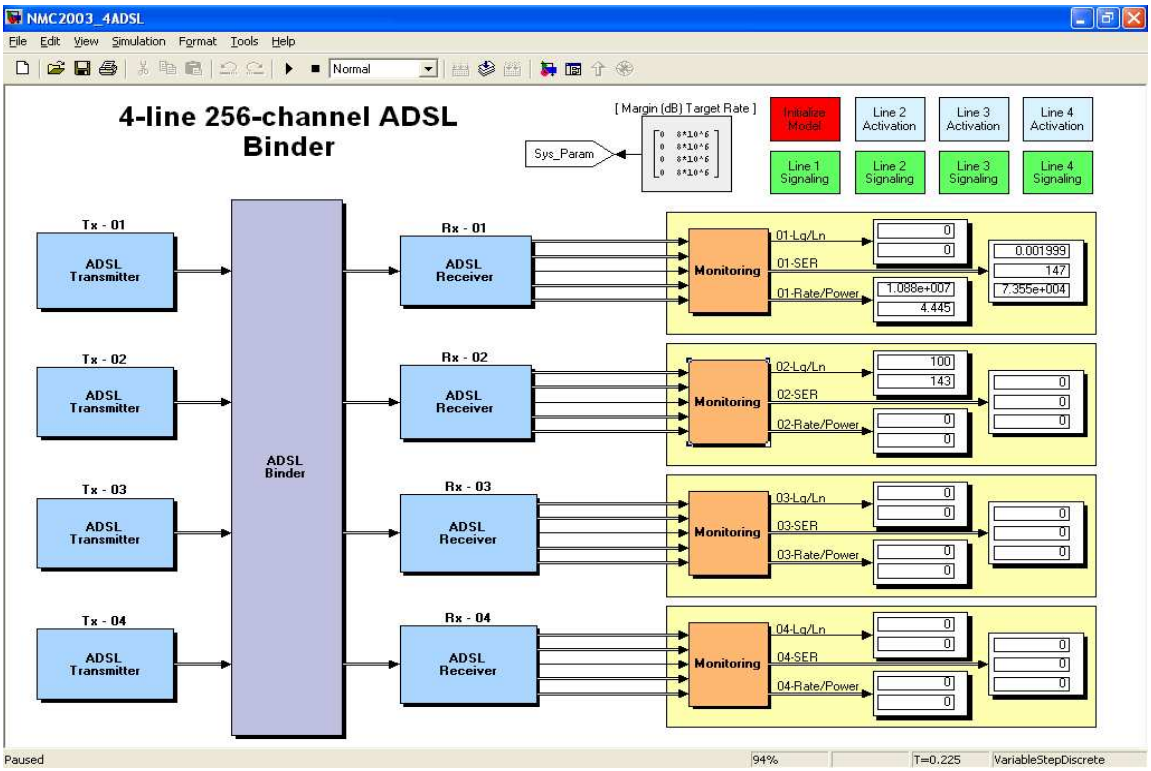

Figure 2. The 4-lines ADSL binder model in Simulink.

performance has become an appealing challenge and consequently *Dynamic Spectrum Management* [6], [7] of the loop plant is the recent trend in DSL industry. Moreover, multicarrier communication has attracted a lot of attention for both wired and wireless communication and DMT is also considered as the transmission method for the very high-bit-rate DSL (VDSL) systems [1]. The ADSL binder model presented in this paper enables the investigation of the multicarrier communication aspects in a noisy environment of multiple transceivers and facilitates the development of centralized algorithms that aim to maximization of the binder system performance.

A key feature of the model architecture is the integration of the simulation environment with a reprogrammable hardware platform and the progressive substitution of different model components with prototype circuit modules. The Simulink environment communicates with a prototype hardware platform via the PCMCIA interface. Selected system components can be mapped into circuit counterparts using a library of custom blocks that provide synchronization and data exchange between the MATLAB workspace and the hardware platform. An embedded dual-port memory unit, accessed by the Simulink and the hardware modules, enables the integration of the simulation model and the hardware prototype into a complete functional system.

The rest of this paper proceeds as follows: Section 2 describes the ADSL binder model and discusses the implementation details of its subsystems. Section 3 describes the integration of the simulation model and the hardware platform and also presents two application examples of implementing an ADSL bit-loading module [8] and a DSL binder emulator on a target digital signal processor (DSP). The hardware implementations of the bit-loading module and the binder emulator are tested using the ADSL binder model under the mixed simulation-hardware environment.

2. The ADSL Binder Model

The Simulink ADSL binder model is shown in Figure 2. It consists of 4 ADSL transceiver-pair subsystems, the subscriber loop binder subsystem and a set of control buttons, that enable the user to activate or deactivate an ADSL line during the simulation or to modify the background noise level. An ADSL line introduces noise to the other lines of the binder only when it has been activated. The model also provides a set of run-time scopes that monitor system and line parameters including bit-error rate, transmit and/or receive power spectrum, modulation bit and gain profiles. For simplicity, in this discussion we consider only the downstream transmission, that is from the CO to the CP.

A key feature of the model architecture is the update of the model block parameters during simulation. This enables the real-time investigation of the system response as a result of a user algorithm or a custom process. This feature along with the "on-the-fly" activation/deactivation of the ADSL lines in the binder determine a dynamic simulation environment for the ADSL binder system.

2.1. The ADSL Transceiver Subsystem

The ADSL transceiver subsystem supports the signaling and the steady-state data transmission mode of operation. Signaling is the link establishment phase of the far-end transceivers before the actual data transmission is performed. During signaling the two modems exchange specific signals and messages in order to train the transceiver circuits and negotiate the communication parameters. The detailed procedures for the signaling protocol in ADSL systems are defined in [2].

In general, during signaling the transceivers train the automatic gain control (AGC), timing recovery and equalizer circuits and perform channel and signal-to-noise ratio (SNR) estimation in order to determine the bit and gain profiles of the multicarrier communication. In the current version of our model, we assume synchronization between transmitter and receiver, which is achieved via suitable timing definition and processing of the sample and frame-based signals of the model blocks. Moreover, the model does not include a time-domain equalizer. In ADSL transmission the time-domain equalizer is used for shortening the channel impulse response (IR) so that the combined channel and equalizer IR is less than the cyclic prefix defined for the DMT frame. The ADSL standard defines a cyclic prefix of 32 samples [2]. Since no time-domain equalizer is used in the model, we increased the cyclic prefix length according to the size of the FIR filter that models the channel IR. This modification results in a relative data rate overhead, but preserves the principles of the DMT signal transmission and reception.

In the current implementation, the signaling mode of the ADSL transceivers incorporates the transmission of the wide-band pseudorandom Medley sequence [2], [9] used by the receiver in order to estimate the SNR of each ADSL subchannel. This information enables the calculation of the bit and gain profiles of the multicarrier communication. The algorithm used to calculate these profiles is known as bit-loading algorithm [8], [10].

In the presented Simulink model, the transmission mode is selected via control signals that are generated automatically during simulation. Initially a new activated line enters the signaling mode of operation. At the end of the Medley sequence, the receiver executes a bit-loading algorithm and calculates the bit and gain profiles for the 256 ADSL

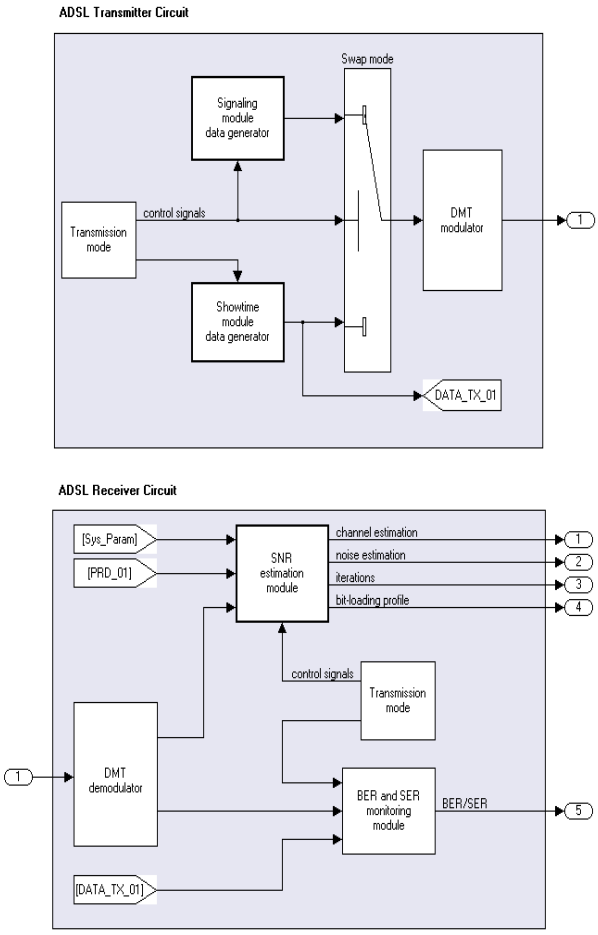

Figure 3. ADSL Tx and Rx subsystems.

subchannels. These distributions automatically update the relative information of the model blocks, so that the simulation is continued with the new parameters. Immediately after finishing the signaling phase, the ADSL transceiver-pair enters the data transmission phase. It should be noted that the activation of each line in the binder is controlled by the user during simulation and therefore the SNR estimation in the signaling mode reflects the noise conditions of the binder at that time.

Figure 3 shows the architecture of the ADSL transmitter (Tx) and receiver (Rx) subsystems. The DMT modulator/demodulator blocks are based on models provided by The Mathworks [11] and incorporate QAM subsymbol encoding/decoding, FFT based modulation/demodulation, gain scaling and framing operations. At the transmitter we can distinguish the signaling and showtime data generator modules along with the transmission mode control block. At the receiver end, there is an SNR estimation module, which is active during signaling and also calculates the bit-loading

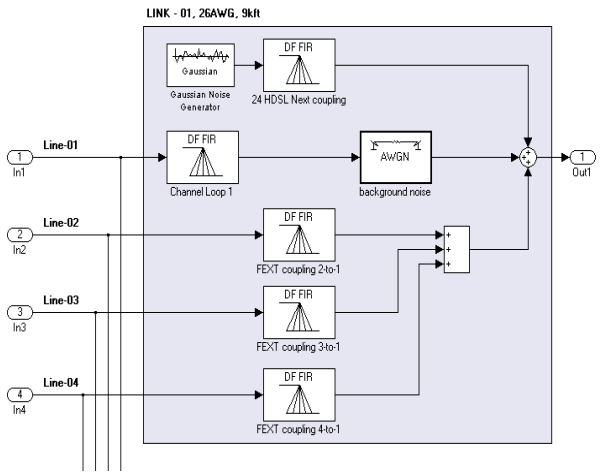

Figure 4. Part of the binder subsystem.

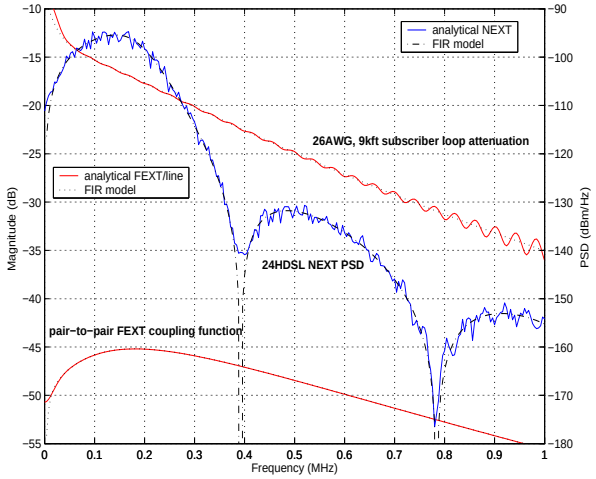

Figure 5. Analytical and FIR model accuracy.

distributions. A bit error rate (BER) monitoring module is also included at the receiver, which enables the visualization of the communication performance during simulation. In case of BER increase in an active ADSL line, the user is able to switch the line in signaling mode so that a new bit-loading profile can be calculated. This process is similar to the response of the modem's supervision unit in case of performance degradation. In the current implementation of the binder model, the ADSL transceiver subsystems do not include forward error correction and other framing operations (e.g. scrambler, crc checksum). The investigation and analysis of the multicarrier aspects of the DSL noise environment can be realized without these functions.

2.2. The Binder Subsystem

The binder subsystem models the DSL binder environment regarding loop attenuation and noise, including thermal AWGN, NEXT crosstalk generated by other DSL sources (e.g. HDSL, ISDN, T1) and FEXT crosstalk between the four ADSL lines. The NEXT sources are modeled as background noise in the binder subsystem using a Gaussian noise generator and a crosstalk shaping filter. The FEXT interference between the ADSL lines is analytically modeled via pair-to-pair coupling functions. We consider that our ADSL modems use frequency division multiplexing (FDM) [1] in order to avoid self-NEXT.

Figure 4 shows the part of the binder subsystem that models the loop and noise environment for the first ADSL link of the general model. The binder corresponds to 9 kft, 26 AWG loops with -140 dBm/Hz AWGN, NEXT crosstalk generated by 24 HDSL lines and analytical FEXT crosstalk generated by the neighboring ADSL lines. Loop attenuation and crosstalk coupling functions are modeled using FIR filters, whose transfer functions correspond to the analytical expressions defined in [12] for DSL systems analysis. We have used 100-tap FIR filters to model both channel loop and crosstalk transfer functions. Figure 5 shows the accuracy of the FIR blocks in relation to the analytical expressions.

3. Simulink Model and Hardware Integration

A key feature of the model architecture is the interaction of the simulation environment with a hardware platform via the PCMCIA interface. This interaction enables the user to develop custom circuits that communicate with the simulation model. Based on a well-defined interface that provides data exchange and synchronization, the user is able to build a mixed-level model that consists of high-level Simulink blocks and low-level circuit modules. The new mixed-level model constitutes a complete functional system that enables simulation of the generic model, while specific functions are executed in circuit prototypes. This integration between the Simulink model and the hardware platform provides a flexible environment for prototyping ADSL and other signal processing circuits [13].

3.1. Hardware Architecture

In order to have an expandable prototyping environment we developed a hardware platform that is based on reprogrammable and reconfigurable devices (FPGAs and DSPs). Figure 6 shows the general mixed-level prototyping setup consisting of the hardware platform and a computer that hosts the Simulink model and communicates with the circuit modules via the PCMCIA interface. In the current version, the platform is based on two Virtex-II FPGAs, having 2 Million gates in total and two TMS320C6711 float-

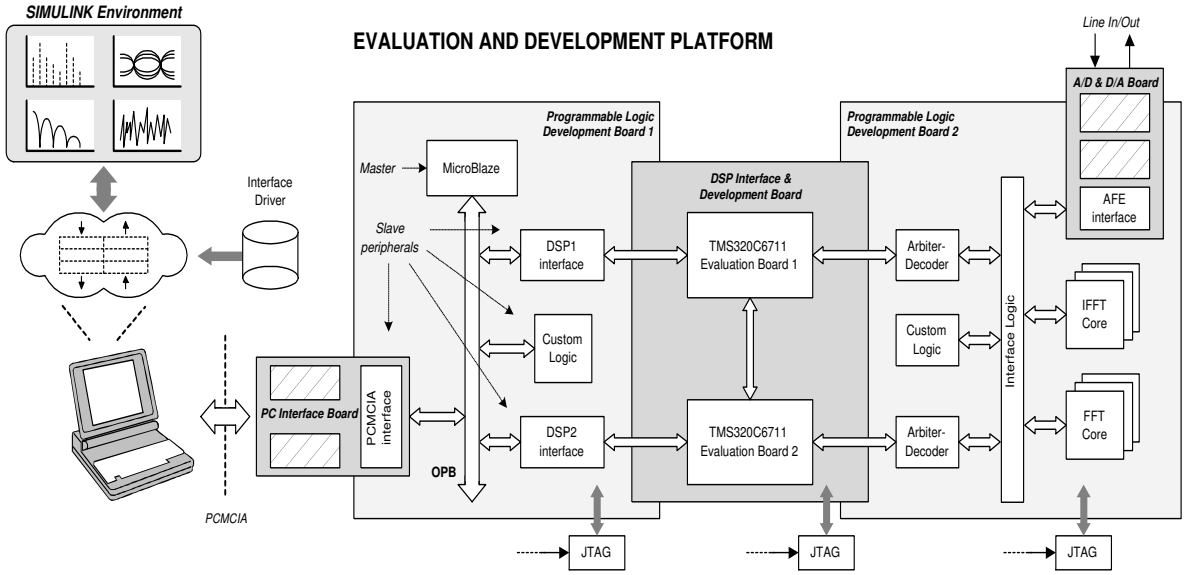

Figure 6. The mixed-level simulation and hardware development setup.

ing point DSPs with 900 MFLOPS processing power. The FPGA and DSP devices are interconnected using a mesh topology, that enables the investigation of several design architectures, while an external analog-front-end (AFE) board with A/D and D/A capabilities is also provided.

Interconnection between the Simulink model and the circuit modules is performed via the PCMCIA interface and a custom FPGA module. The latter provides the necessary circuits for the PCMCIA data transactions and for extending the available I/O memory space. Moreover it includes a dual-port memory (DPRAM), that is accessed by both the Simulink blocks and the hardware modules and contains all necessary user and control information for the mixed-model data flow. In the block diagram of Figure 6 we present a system architecture that is based on the MicroBlaze processor [14] and the IBM's industry standard On-chip Peripheral Bus (OPB) [15] for developing the circuit modules. MicroBlaze is the master device and all other circuit modules are developed as peripheral OPB devices. Using the topology depicted in Figure 6 the user has the flexibility to design a system architecture that meets the specific application requirements. When the circuit modules are entirely developed on the 6711 DSP processor, the architecture can be simplified by directly interfacing the DSP to the PCMCIA FPGA module. Figure 7 shows the actual prototyping platform and its interconnection with a host computer.

3.2. Prototyping Examples

The mixed-level prototyping setup of the ADSL binder model with the hardware platform has been used for the development of a bit-loading circuit module and a hardware DSL binder emulator.

As described in subsection 2.1, the transmission at each ADSL line is based on the bit-loading profiles calculated during the signaling phase. In the Simulink model we replace the bit-loading functions with a custom library that provides access to the PCMCIA driver, so that the receivers' SNR estimation modules in Figure 3 communicate with the DPRAM in the hardware platform. The bit-loading function is then implemented in the floating point 6711 DSP as an independent software module for each ADSL line of our model. At the end of the signaling phase, the SNR values along with line parameters, including target data rate and system margin, are transferred from the MATLAB workspace to the DPRAM and then to the DSP device. When the bit and gain distributions are ready, the DSP transfers the data to the DPRAM and the Simulink library updates the corresponding vectors in the model blocks. The simulation continues with the new bit-loading profile and the effect of the implementation can be demonstrated via the simulation results. Synchronization between the simulation progress and the DSP execution time is maintained through suitable control data exchange.

The mixed-level prototyping setup has also been used for the development of a hardware DSL binder emulator. The emulator is executed on the floating point 6711 DSP and emulates the noise environment of the DSL binder. The Simulink model consists of one full ADSL line and a crosstalk traffic generator. The traffic generator reads prestored data that correspond to crosstalk disturbing lines in the binder including T1, ISDN, HDSL and ADSL transmission. The ADSL signal and the crosstalk data are trans-

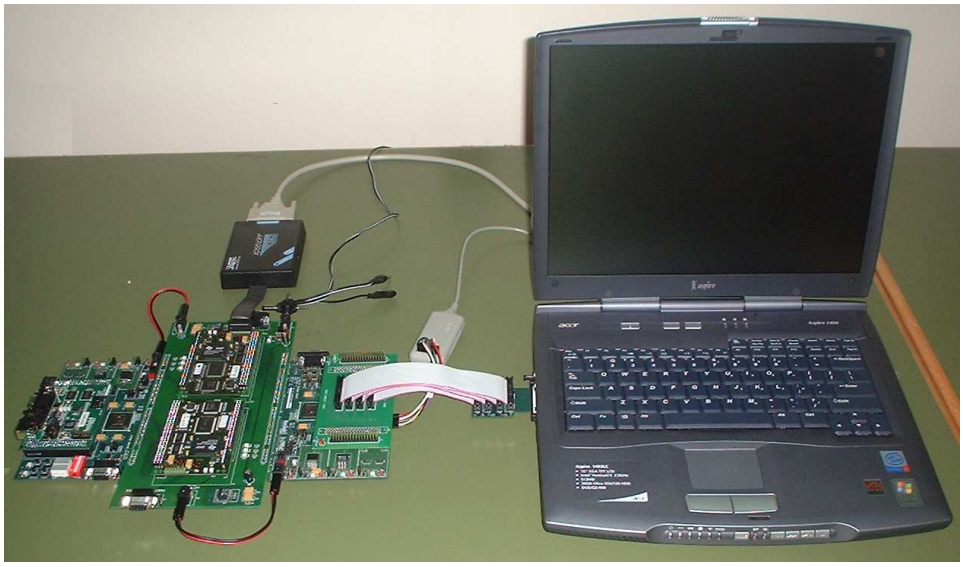

Figure 7. The prototyping hardware platform.

ferred to the DSP. Based on a library of standard test-loops and analytical expressions for crosstalk coupling functions, the DSP binder emulation module calculates the binder output regarding line attenuation and crosstalk interference. The output signal values are returned to the Simulink model and are fed back to the ADSL receiver subsystem.

4. Conclusions

In this paper we presented a simulation model of a binder of ADSL lines developed in the Simulink environment. The simulation model interacts with a reprogrammable hardware platform via a library of custom blocks, thus enabling the substitution of selected model components with hardware and/or software modules. The mixed-level setup of the ADSL binder model with the hardware platform constitutes a versatile environment for the development and prototyping of new single-modem and centralized algorithms for the ADSL technology.

5. Acknowledgments

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